EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	4944	438/244,253,396,630,649.ccls.	US-PGPUB; USPAT	OR	ON	2007/03/03 12:40
L4	3880	3 and @ad<"20030312"	US-PGPUB; USPAT	OR	ON	2007/03/03 12:44
L5	810	4 and (CMOS or PMOS or NMOS or NMOSFET or PMOSFET)	US-PGPUB; USPAT	OR	ON	2007/03/03 12:42
L6	860	4 and (CMOS or PMOS or NMOS or (N near3 MOSFET) or (P near3 MOSFET))	US-PGPUB; USPAT	OR	ON	2007/03/03 12:43
L7	32	(denise with m with eppich) or (ronald with a with weimer) and (CMOS or PMOS or NMOS or (N near3 MOSFET) or (P near3 MOSFET))	US-PGPUB; USPAT	OR	ON	2007/03/03 12:45
L8	14	7 and @ad<"20030312"	US-PGPUB; USPAT	OR	ON	2007/03/03 12:47
L9	0	(denise with m with eppich) or (ronald with a with weimer) and (CMOS or PMOS or NMOS or (N near3 MOSFET) or (P near3 MOSFET))	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/03 12:45
L10	331	((CMOS or PMOS or NMOS or (N near3 MOSFET) or (P near3 MOSFET)) and metal and silicon and (doped or implanted) and thickness).clm.	US-PGPUB; USPAT	OR	ON	2007/03/03 12:46
L11	214	10 and @ad<"20030312"	US-PGPUB; USPAT	OR	ON	2007/03/03 12:47

DOCUMENT-IDENTIFIER: US 20040063264 A1

TITLE: Method of forming a high performance and low cost CMOS device

---------- KWIC ---------

Claims Text - CLTX (2):

1. A method of fabricating a complimentary **metal** oxide semiconductor (CMOS) device on a semiconductor substrate, comprising the steps of: providing a first device region of said semiconductor substrate to accommodate a first conductivity type device, and providing a second device region of said semiconductor substrate to accommodate a second conductivity type device; forming gate structures on an underlying gate insulator layer in said first device region, and in said second device region; forming insulator structures comprised of a thick insulator component located on the sides of said gate structures and on a first portion of the semiconductor substrate located adjacent to said gate structure, and comprised of a thin insulator component located on a second portion of said semiconductor substrate in turn located adjacent to the thick insulator component overlying said first portion of said semiconductor substrate; performing a first series of ion implantation procedures in said first device region to form a first halo region of a first conductivity type in said first portion of said semiconductor substrate, in said second portion of said semiconductor substrate, and in a portion of said semiconductor substrate underlying an edge of said gate structure, and to form a first lightly doped source/drain (LDD) region of a second conductivity type in a top portion of said halo region underlying said thick insulator component, and to form a first heavily doped source/drain region of a second conductivity type in a top portion of said halo region located underlying said thin insulator component located overlying said second portion of said semiconductor substrate; performing a second series of ion implantation procedures in said second device region to form a second halo region of a second conductivity type in a first portion of said semiconductor substrate, in a second portion of said semiconductor substrate, and in a portion of said semiconductor substrate underlying an edge of said gate structure, and to form a second lightly doped source/drain (LDD) region of a first conductivity type in a top portion of said halo region underlying said thick insulator component, and to form a second heavily doped source/drain region of a first conductivity type in a top portion of said halo region underlying said thick insulator component located overlying said second portion of said semiconductor substrate; forming insulator shapes

on said insulator structure located in said first device region resulting in a composite insulator spacer on gate structure exposing top surface of said gate structure and exposing top surface of said second heavily doped source/drain region; and forming **metal** silicide on exposed said top surface of said gate structure and on top surface of said first heavily doped source/drain region.

Claims Text - CLTX (3):
2. The method of claim 1, wherein said first device region is an N channel **metal** oxide semiconductor (NMOS), device.

Claims Text - CLTX (4):
3. The method of claim 1, wherein said first device region is a P channel **metal** oxide semiconductor (PMOS), device.

Claims Text - CLTX (5):
4. The method of claim 1, wherein said second device region is an N channel **metal** oxide semiconductor (NMOS), device.

Claims Text - CLTX (6):
5. The method of claim 1, wherein said second device region is a P channel **metal** oxide semiconductor (PMOS), device.

Claims Text - CLTX (7):
6. The method of claim 1, wherein said gate insulator layer is a silicon dioxide layer obtained via thermal oxidation procedures at a **thickness** between about 10 to 100 Angstroms.

Claims Text - CLTX (8):
7. The method of claim 1, wherein said gate structures, at a **thickness** between about 1000 to 3000 Angstroms, are comprised of doped polysilicon, or polycide wherein the polycide is comprised of **metal** silicide on polysilicon.

Claims Text - CLTX (9):
8. The method of claim 1, wherein said insulator structure is comprised of silicon oxide, featuring a thick insulator component at a **thickness** between about 200 to 400 Angstroms, and featuring a thin insulator component at a **thickness** between about 150 to 350 Angstroms.

Claims Text - CLTX (14):
13. The method of claim 1, wherein said insulator shapes are comprised of silicon nitride, at a **thickness** between about 200 to 800 Angstroms.

Claims Text - CLTX (15):

14. The method of claim 1, wherein said **metal** silicide is chosen from a group that contains titanium silicide, tantalum silicide, tungsten silicide, nickel silicide, cobalt silicide, and zirconium silicide.

Claims Text - CLTX (16):

15 A method of fabricating a CMOS device on a semiconductor substrate, comprising the steps of: providing a first portion of said semiconductor substrate as an N channel **metal** oxide semiconductor (NMOS) region, to accommodate an NMOS device, and providing a second portion of said semiconductor substrate as a P channel **metal** oxide semiconductor (PMOS) region to accommodate a PMOS device; growing a silicon dioxide gate insulator on said semiconductor substrate; forming gate structures on said silicon dioxide gate insulator layer; depositing a silicon oxide layer; depositing a first silicon nitride layer; performing a first anisotropic reactive ion etch (RIE), procedure to form first composite insulator spacers on the sides of said gate structures, comprised of first silicon nitride shapes on underlying thick silicon oxide shapes, overlying first portions of said semiconductor substrate, and with thin silicon oxide shapes, not covered by said gate structures or by said first composite insulator spacers, formed overlying second portions of said semiconductor substrate; removing said first silicon nitride shapes resulting in an L shaped silicon oxide spacer comprised of said thick silicon oxide shape on sides of said gate structure and overlying said first portions of said semiconductor substrate, and with said L shaped silicon oxide spacer comprised of said thin silicon oxide shapes overlying said second portions of said semiconductor substrate; forming a first block out shape in said PMOS region; performing a first series of ion implantation procedures in said NMOS region to form a P type halo region in said first portion of said semiconductor substrate, in said second portion of said semiconductor substrate, and in a third portion of said semiconductor substrate located underlying an edge of said gate structure, and to form an N type lightly doped source/drain (LDD) region in a top portion of said P type halo region underlying said thick silicon oxide shape, and to form an N type heavily doped source/drain region in a top portion of said P type halo region located underlying said thin silicon oxide shape; forming a second block out shape in said NMOS region; performing a second series of ion implantation procedures in said PMOS region device region to form an N type halo region in a first portion of said semiconductor substrate, in a second portion of said semiconductor substrate, and in a third portion of said semiconductor substrate underlying an edge of said gate structure, and to form a P type LDD region in a top portion of said N type halo region underlying said thick silicon oxide shape, and to form a P type heavily doped source/drain region in a top portion of said N type halo region located

underlying said thin silicon oxide shape; depositing a second silicon nitride layer; performing a second anisotropic RIE procedure resulting in a second composite insulator spacer in said NMOS region, comprised of said second silicon nitride shapes on said thick silicon oxide shapes of said L shaped silicon oxide spacer, and exposing top surface of said N type heavily doped source/drain region, while second silicon nitride layer in said PMOS region remains unetched; and forming **metal** silicide on said top surface of said gate structure and on top surface of said N type heavily doped source/drain region, in said NMOS region.

Claims Text - CLTX (17):
16. The method of claim 15, wherein said silicon dioxide gate insulator layer is obtained via thermal oxidation procedures at a **thickness** between about 10 to 100 Angstroms.

Claims Text - CLTX (18):
17. The method of claim 15, wherein said gate structures are defined with a **thickness** between about 1000 to 3000 Angstroms, comprised of doped polysilicon, or polycide, wherein the polycide is comprised of **metal** silicide on polysilicon.

Claims Text - CLTX (19):
18. The method of claim 15, wherein said silicon oxide layer is obtained at a **thickness** between about 200 to 400 Angstroms via LPCVD or PECVD procedures.

Claims Text - CLTX (20):
19. The method of claim 15, wherein said first silicon nitride layer is obtained at a **thickness** between about 500 to 800 Angstroms via LPCVD or PECVD procedures.

Claims Text - CLTX (21):
20. The method of claim 15, wherein the **thickness** of said thin silicon oxide shapes of said L shaped silicon oxide spacer are between about 150 to 350 Angstroms, while the **thickness** of the unetched thick silicon oxide shapes are between about 200 to 400 Angstroms.

Claims Text - CLTX (27):
26. The method of claim 15, wherein said second silicon nitride layer is obtained via LPCVD or PECVD procedures, at a **thickness** between about 200 to 800 Angstroms.

Claims Text - CLTX (28):

27. The method of claim 15, wherein said **metal** silicide is chosen from a group that contains titanium silicide, tantalum silicide, tungsten silicide, nickel silicide, cobalt silicide, and zirconium.

US-PAT-NO: 6468851

DOCUMENT-IDENTIFIER: US 6468851 B1
See image for Certificate of Correction

TITLE: Method of fabricating CMOS device with dual gate electrode

--------- KWIC ---------

Claims Text - CLTX (1):

1. A method of fabricating a dual gate electrode CMOS device, comprising the steps of: providing a wafer having an N-MOSFET region and a P-MOSFET region; forming a sacrificial gate layer/doped N.sup.+ poly-1 layer/gate insulator layer stack over the wafer; patterning the N-MOSFET sacrificial gate layer to form a once patterned sacrificial gate layer only within the N-MOSFET region, exposing the doped N.sup.+ poly-1 layer within the P-MOSFET region; forming an undoped poly-2 layer over the once patterned sacrificial gate layer and the exposed N.sup.+ poly-1 layer within the P-MOSFET region; planarizing the undoped poly-2 layer to form a planarized undoped poly-2 layer only within the P-MOSFET region; patterning: the once patterned sacrificial gate layer, the doped N.sup.+ poly-1 layer and the gate insulator layer within the N-MOSFET region to form an initial N-MOSFET gate electrode stack having exposed sidewalls; and the planarized undoped poly-2 layer, the doped N.sup.+ poly-1 layer and the gate insulator layer within the P-MOSFET region to form an initial P-MOSFET gate electrode stack having exposed sidewalls; forming sidewall spacers adjacent the exposed sidewalls of the initial N-MOSFET and P-MOSFET gate electrode stacks; forming an intermetal dielectric layer adjacent and between the initial N-MOSFET and P-MOSFET gate electrode stacks; removing the initial P-MOSFET gate electrode stack to form a P-MOSFET gate cavity exposing a portion of the wafer; forming a second P-MOSFET gate insulator layer within the P-MOSFET gate cavity over the exposed portion of the wafer; removing the upper sacrificial gate layer of the initial N-MOSFET gate electrode stack to form an N-MOSFET gate cavity; forming a **metal** layer over the structure, filling the remaining P-MOSFET gate cavity and the N-MOSFET gate cavity; and planarizing the **metal** layer to remove the excess **metal** from over the intermetal dielectric layer leaving planarized **N-MOSFET metal** gate electrode cap within N-MOSFET gate cavity to form a finalized **N-MOSFET and planarized P-MOSFET metal** gate within the remaining P-MOSFET gate cavity to form a finalized P-MOSFET, thus completing formation of the dual gate electrode

CMOS device.

Claims Text - CLTX (11):
11. The method of claim 1, wherein the second P-MOSFET gate insulator layer has a **thickness** of from about 10 to 200 .ANG..

Claims Text - CLTX (13):
13. The method of claim 1, wherein the **metal** layer is comprised of a material selected from the group consisting of copper, aluminum, titanium nitride and tungsten.

Claims Text - CLTX (14):
14. The method of claim 1, wherein the **metal** layer is copper.

Claims Text - CLTX (15):
15. A method of fabricating a dual gate electrode CMOS device, comprising the steps of: providing a wafer having an N-MOSFET region and a P-MOSFET region; forming a sacrificial gate layer/doped N.sup.+ poly-1 layer/gate insulator layer stack over the wafer; patterning the N-MOSFET sacrificial gate layer to form a once patterned sacrificial gate layer only within the N-MOSFET region, exposing the doped N.sup.+ poly-1 layer within the P-MOSFET region; forming an undoped poly-2 layer over the once patterned sacrificial gate layer and the exposed N.sup.+ poly-1 layer within the P-MOSFET region; planarizing the undoped poly-2 layer to form a planarized undoped poly-2 layer only within the P-MOSFET region; patterning: the once patterned sacrificial gate layer, the doped N.sup.+ poly-1 layer and the gate insulator layer within the N-MOSFET region to form an initial N-MOSFET gate electrode stack having exposed sidewalls; and the planarized undoped poly-2 layer, the doped N.sup.+ poly-1 layer and the gate insulator layer within the P-MOSFET region to form an initial P-MOSFET gate electrode stack having exposed sidewalls; forming respective conventional LDD implants within the wafer adjacent the initial N-MOSFET and P-MOSFET gate electrode stacks; forming sidewall spacers adjacent the exposed sidewalls of the initial N-MOSFET and P-MOSFET gate electrode stacks; forming respective S/D implants adjacent the respective LDD implants; forming respective silicide portions on the wafer over the respective S/D implants; forming an intermetal dielectric layer adjacent and between the initial N-MOSFET and P-MOSFET gate electrode stacks; removing the initial P-MOSFET gate electrode stack to form a P-MOSFET gate cavity exposing a portion of the wafer; forming a second P-MOSFET gate insulator layer within the P-MOSFET gate cavity over the exposed portion of the wafer; removing the upper sacrificial gate layer of the initial N-MOSFET gate electrode stack to form an N-MOSFET gate cavity; forming a **metal** layer over the structure, filling the

remaining P-MOSFET gate cavity and the N-MOSFET gate cavity; and planarizing the **metal** layer to remove the excess **metal** from over the intermetal dielectric layer leaving planarized **N-MOSFET metal** gate electrode cap within N-MOSFET gate cavity to form a finalized **N-MOSFET and planarized P-MOSFET metal** gate within the remaining P-MOSFET gate cavity to form a finalized P-MOSFET, thus completing formation of the dual gate electrode CMOS device.

Claims Text - CLTX (24):
24. The method of claim 15, wherein the second P-MOSFET gate insulator layer has a **thickness** of from about 10 to 200 .ANG..

Claims Text - CLTX (26):
26. The method of claim 15, wherein the **metal** layer is comprised of a material selected from the group consisting of copper, aluminum, titanium nitride and tungsten.

Claims Text - CLTX (27):
27. The method of claim 15, wherein the **metal** layer is copper.

Claims Text - CLTX (28):
28. A method of fabricating a dual gate electrode CMOS device, comprising the steps of: providing a wafer having an N-MOSFET region and a P-MOSFET region; forming a sacrificial gate layer/doped N.sup.+ poly-1 layer/gate insulator layer stack over the wafer; the sacrificial gate layer being formed of a material selected from the group consisting of silicon nitride and nitride; the gate insulator layer is formed of a material selected from the group consisting of silicon oxide or a high-k dielectric material; patterning the N-MOSFET sacrificial gate layer to form a once patterned sacrificial gate layer only within the N-MOSFET region, exposing the doped N.sup.+ poly-1 layer within the P-MOSFET region; forming an undoped poly-2 layer over the once patterned sacrificial gate layer and the exposed N.sup.+ poly-1 layer within the P-MOSFET region; planarizing the undoped poly-2 layer to form a planarized undoped poly-2 layer only within the P-MOSFET region; patterning: the once patterned sacrificial gate layer, the doped N.sup.+ poly-1 layer and the gate insulator layer within the N-MOSFET region to form an initial N-MOSFET gate electrode stack having exposed sidewalls; and the planarized undoped poly-2 layer, the doped N.sup.+ poly-1 layer and the gate insulator layer within the P-MOSFET region to form an initial P-MOSFET gate electrode stack having exposed sidewalls; forming respective conventional LDD implants within the wafer adjacent the initial N-MOSFET and P-MOSFET gate electrode stacks; forming sidewall spacers adjacent the exposed sidewalls of the initial N-MOSFET and P-MOSFET gate electrode stacks; forming respective S/D implants adjacent the

respective LDD implants; forming respective silicide portions on the wafer over the respective S/D implants; forming an intermetal dielectric layer adjacent and between the initial N-MOSFET and P-MOSFET gate electrode stacks; removing the initial P-MOSFET gate electrode stack to form a P-MOSFET gate cavity exposing a portion of the wafer; forming a second P-MOSFET gate insulator layer within the P-MOSFET gate cavity over the exposed portion of the wafer; removing the upper sacrificial gate layer of the initial N-MOSFET gate electrode stack to form an N-MOSFET gate cavity; forming a **metal** layer over the structure, filling the remaining P-MOSFET gate cavity and the N-MOSFET gate cavity; and planarizing the **metal** layer to remove the excess **metal** from over the intermetal dielectric layer leaving planarized **N-MOSFET metal** gate electrode cap within N-MOSFET gate cavity to form a finalized **N-MOSFET and planarized P-MOSFET metal** gate within the remaining P-MOSFET gate cavity to form a finalized P-MOSFET, thus completing formation of the dual gate electrode CMOS device.

Claims Text - CLTX (36):
36. The method of claim 28, wherein the second P-MOSFET gate insulator layer has a **thickness** of from about 10 to 200 .ANG..

Claims Text - CLTX (38):
38. The method of claim 28, wherein the **metal** layer is comprised of a material selected from the group consisting of copper, aluminum, titanium nitride and tungsten.

Claims Text - CLTX (39):
39. The method of claim 28, wherein the **metal** layer is copper.